In the United States Patent and Trademark Office

In re application of:	:
Kent	:Art Unit: 2676
AN 10/086,980	:Examiner: Tung, Kee M.
Filed: 03/01/2002	:Atty's Docket: TD-168

For: Yield Enhancement of Complex Chips (confirmation no. 6304)

REPLY BRIEF

Honorable Commissioner of Patents and Trademarks
Alexandria, VA 22313

Sir:

Appellant respectfully submits the following Reply to the new arguments presented in Examiner Tung's Answer mailed 05/04/2005.

RESPONSE TO NEW ARGUMENTS

In his answer to the appeal brief filed on 03/04/2005, Examiner Tung raises the following new arguments:

I. Appellant is not arguing over terminology.

Examiner Tung has suggested that, "*Basically, appellant argues the terminology used in the Prior Art, such as, processor vs an unit.*" This is incorrect. What Appellant does assert is that physically removing a defective processor from a plurality of queue processors is not the same thing as salvaging the defective processor by bypassing any defective pipelines within that processor. Brent *et al.* do not teach the problem or source of improving the yield enhancement of complex, integrated circuit chips.

Examiner Tung also appears to suggest that Appellant simply regards a processor as a larger scale component than a unit. This is also incorrect. Again, what Appellant does assert is that physically removing a defective processor from a plurality of queue processors is not the same thing as salvaging the defective processor by bypassing any defective pipelines within that processor.

Examiner Tung also suggests, "*By the way, if a 'single' graphics processor comprising a plural computational units and each unit includes multiple vertex processors, then the 'single' graphics processor is considered as a 'multiple' processor.*" Appellant would like to point out that in that situation, you would still have **a single graphics processor** but with multiple **vertex** processors. You would not have multiple **graphics** processors. There is a significant difference.

With regard to the Pentium 4 processor, Examiner Tung has suggested that, "*a Pentium 4 processor is labeled a single processor but contains multiple processors.*" However, the product description of the Pentium 4 processor at http://www.intel.com/design/pentium4/prodbref/ states:

> HT Technology is ground-breaking technology that changes the landscape of processor design by going beyond GHz to improve processor performance. It allows software programs to "see" two processors and work more efficiently. This new technology enables the processor to

> execute two series, or threads, of instructions at the same time, thereby improving performance and system responsiveness.

Therefore, even with HT technology, a single Pentium 4 processor can only execute two threads of instructions at a time. Clearly, this would not be the case if there were multiple processors as Examiner Tung claims. The Pentium 4 processor would be able to execute multiple threads of instructions simultaneously, not just two, if Examiner Tung's suggestion were correct.

Accordingly, the multiple vertex processors of claim 3 are not contradicted by Appellant's arguments.

Examiner has also suggested that, "*It is well known and well used in the patent applications, specially in patent claims, a processor, a computation unit, a processing unit, and a controller, etc. ... are interchangeable in the art and all can be called as a processor. Each can vary in size and the scale of the components can all be different.*" Again, Appellant is not arguing over terminology. Appellant is stating that salvaging a defective processor by bypassing any defective pipelines within that processor is not taught or suggested by physically removing a defective processor from a plurality of queue processors.

II. Brent *et al.* do not bypass a defective unit. They physically remove it from the configuration.

Examiner Tung has suggested, "*In the present application, the important issue is what the Brent reference as a whole teaches to one of ordinary skill in the art (allocation between multiple processors/units) in place of Baldwin.*" Appellant could not agree more. What Brent *et al.* teach is an ADM recovery feature whereby:

> *the failing processor is stopped, removed from the operational subsystem, and its work redistributed to other processors through the subsystem workload balancing process. ...*
> *This invention also provides an ADM dynamic reconfiguration feature available for use at any time to allow any processor to be removed, or a new processor to be added, to the subsystem, as long as there is at least one operational processor remaining in the subsystem. (col. 5, line 49 - col. 6, line 17.)*

Brent *et al.* physically remove a failing processor and physically reconfigure the operational subsystem. Clearly, there is no bypassing of a defective unit if the defective unit is physically removed from the operational subsystem. Examiner Tung has correctly noted on page 2 of his office action mailed 08/05/2004 that, "*However, Baldwin fails to explicitly teach or suggest one or more task allocation units programmed to bypass defective ones of said subunits within said groups, and distribute incoming tasks only among operative ones of said subunits.*"

Therefore, none of the applied references, singly or in any motivated combination thereof, discloses or suggests **bypassing** defective units within a group. By contrast, all of the independent claims on appeal claim, among other things, either "one or more task allocation units programmed to bypass defective ones of said units within said groups", or "bypassing defective ones of said units".

Therefore, even if one were motivated to make the suggested combination (which Appellant strongly disputes), it still would not be enabling of the present inventions. Instead, it would result in a process or system whereby a single chip is taken apart to physically remove a failing pipeline in order to reconfigure the chip. This is NOT economically feasible. This fact was highlighted in the following passage from the original application:

> During testing a single bit error anywhere on the die will force that die to be scrapped... This [innovation] allows us to take die which would otherwise be classified as scrap and use them in a lower performance product.
>
> **Figure 1** shows an example of the physical layout of a graphics processing integrated circuit wherein a subset of working parts can define a secondary lower performance part. In this example, if all components are functional, the chip will operate with: 16 vertex processors, 4 texture pipes, 2 memory controllers, and 2 RAMDACs...
>
> However, if some of these components are defective, the same chip can be specified under a secondary part specification, with e.g. as little as 4 vertex processors, 1 texture pipe, 1 memory controller, and 1 RAMDAC.
>
> The results of testing at manufacture can be recorded in any of a variety of known way, e.g. by blowing fuses or by selective laser heating to cause diode punchthrough.
>
> (Page 6, Line 9 - Page 7, line 9).

As established by the section cited above, the present inventions do not require physically removing a defective pipeline from within a graphics processor and reconfiguring that graphics processor before it can be used. Defective pipelines within the graphics processor are simply bypassed, thereby improving the yield enhancement of complex, integrated circuit chips that would otherwise be scrapped.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections.

Respectfully submitted,

05/31/05

Date

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

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Filing Date	March 1, 2002
First Named Inventor	Osman Kent
Art Unit	2676
Examiner Name	Tung, Kee M.
Attorney Docket Number	TD-168

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☑ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
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Remarks

Submission of Reply Brief

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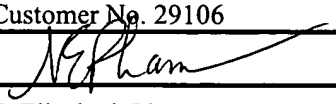
Signature			
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